Use Models for Extending IEEE 1687 to Analog Test

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Peter Sarson

Jeff Rearick

Acknowledgments – in no particular order

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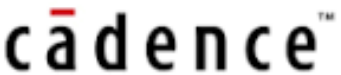
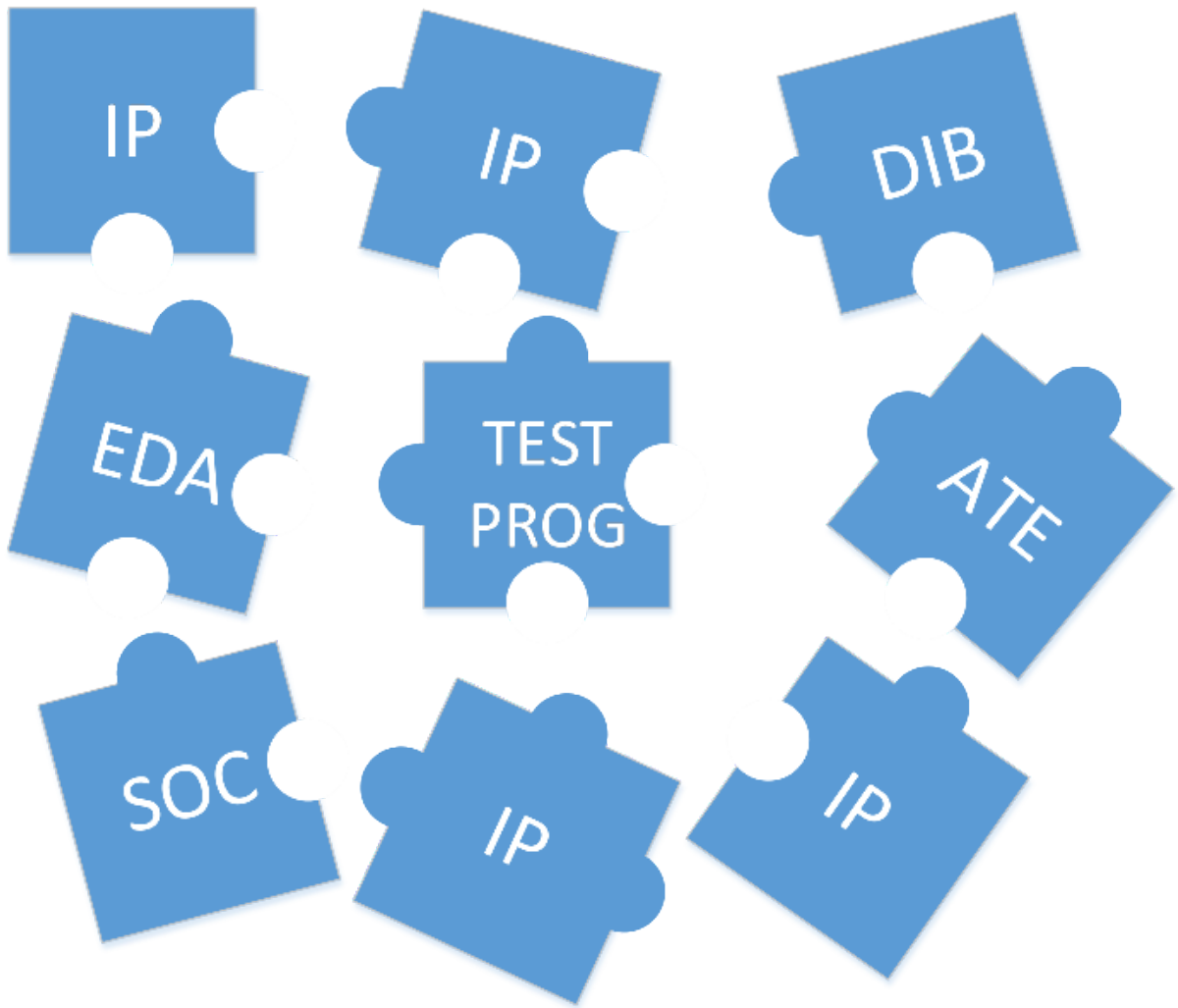


Todays Disconnected Ecosystem



Purpose

- How the proposed IEEE 1687 can be extended to differing complexities of analog and mixed-signal chips.
- How the proposed IEEE 1687 can be extended across the ecosystem of the full chip process to also include ATE.
- What implications these use models have on the 1687 PDL and ICL languages.
  - New commands

Outline

- Show 4 use cases of analog 1687 with examples
- Describe 9 extensions/additions to PDL to form (A)PDL
- Describe extensions to ICL language to extend capabilities to ATE, Including the associated PDL
- Future EDA ecosystem

Introduction

- **Todays IEEE 1687 is**
  - Aimed at digital circuitry – builds upon 1500 to access onboard instruments via SCAN registers
  - ***Mainly digital but does not exclude analog***
- **Analog Test has been a longstanding problem in the industry**
  - No standardization, no EDA automation
  - No linkage from Design to ATE
  - Pretty much a fully manual process

Introduction

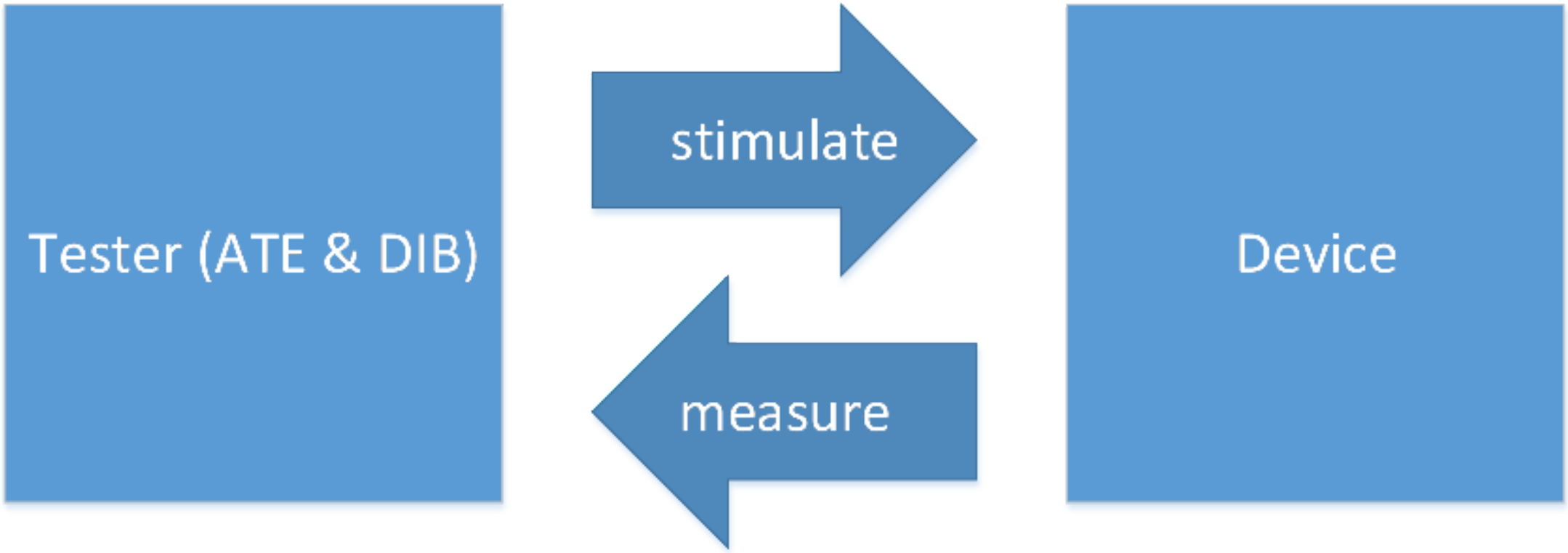
- There is a clear need for improving the development and bring up for analog tests.

- A structured method, which facilitates pattern re-use would be beneficial

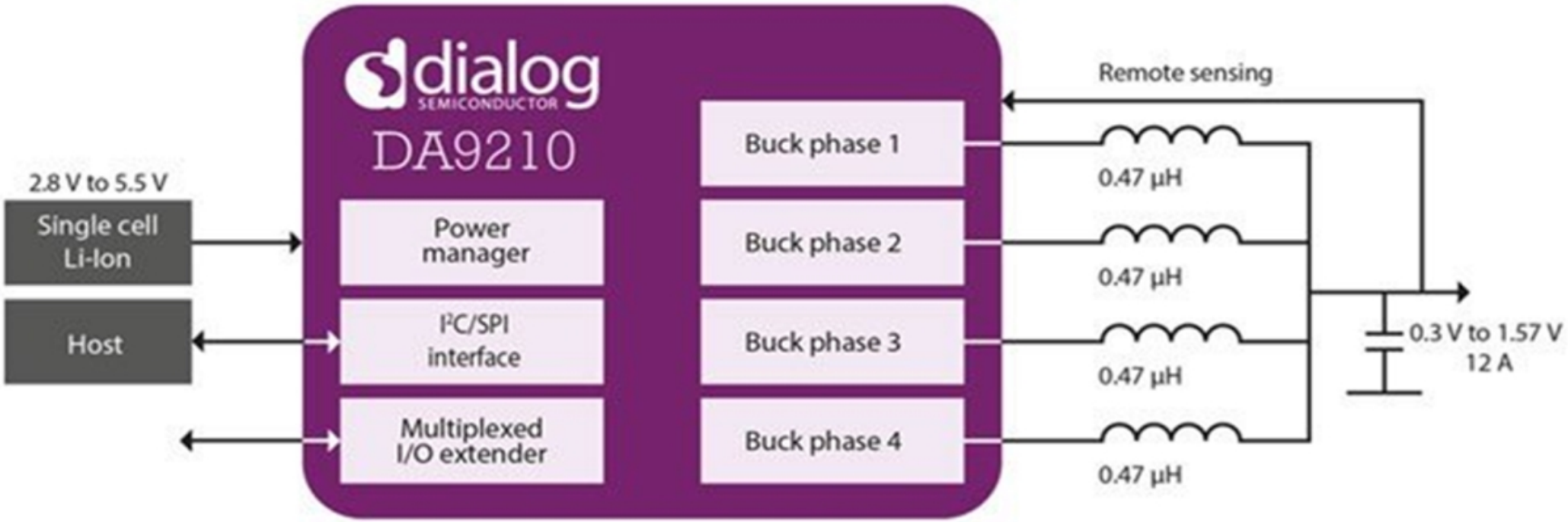
Analog/Mixed Signal Use Model Overview

- I will now present 4 use models based on the ecosystem of how tests are applied to Analog Mixed Signal Devices

Use Model 1 - Classical



Use Model 1 - Classical



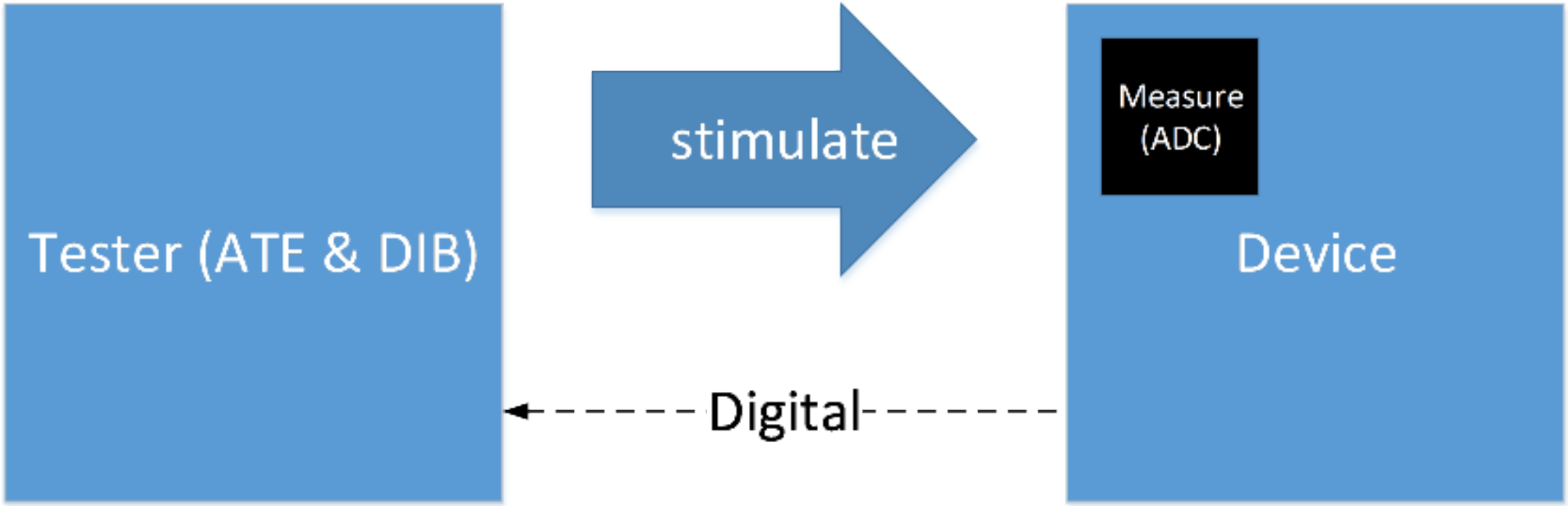
Use Model 1 - Classical

- All though a power converter would not be the 1st thought for a 1687 application.
- Description of ATE instrument in ICL and PDL would allow
  - Programming of ATE instruments with standardized code that could be leveraged for device IP blocks and easily ported between design
  - **Produce a go to standard for analog test writing in PDL**

Use Model 1 - Classical

- **No design information of ATE instruments needed.**
- Simply provide the ports and register information necessary for a test to utilize them using ICL.
  - Implementation by either test writer or retargeting tool

Use Model 2 - DUT has some instruments



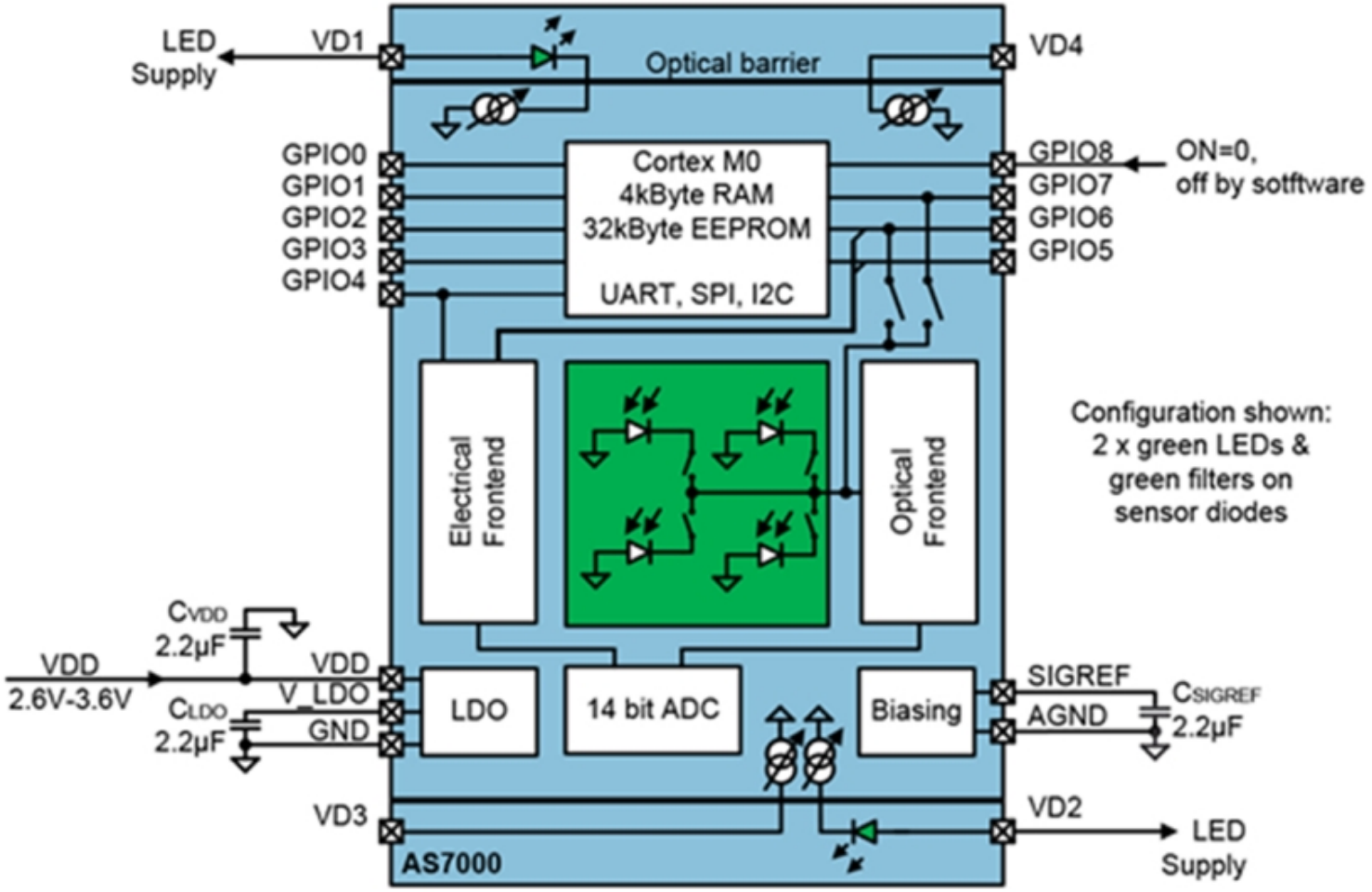
Use Model 2 - DUT has some instruments

- Mixed-signal chips may contain on-chip arbitrary waveform generators, DACs
- Analog circuits may be connected to on-chip measurement instruments e.g. comparators, ADCs, time counters
- All with a digital interface either to program or readout the result

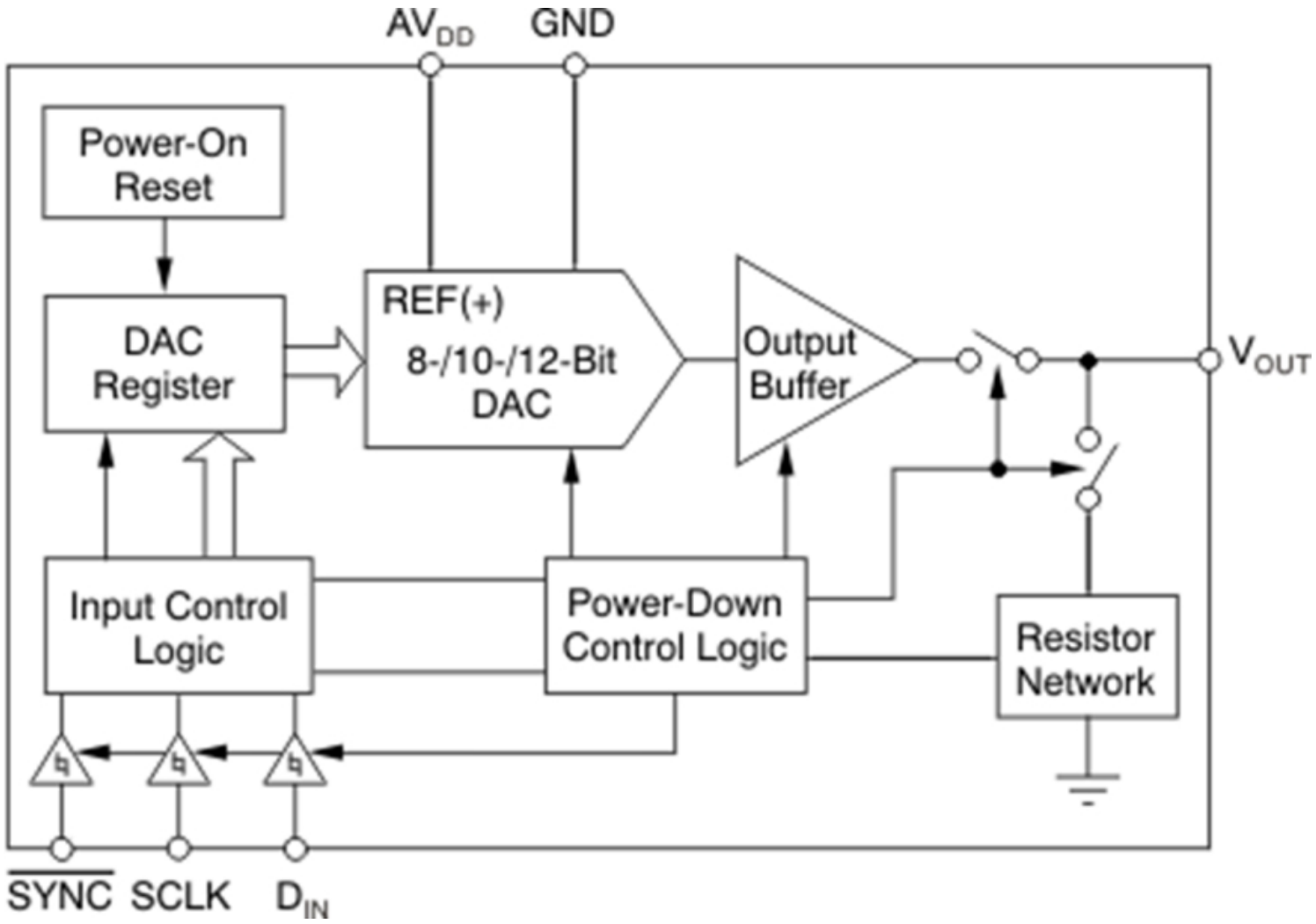
Use Model 2 - DUT has some instruments

- **Both examples need Analog ATE, to either Stimulate or Measure**

Use Model 2 - Examples



Use Model 2 - Examples

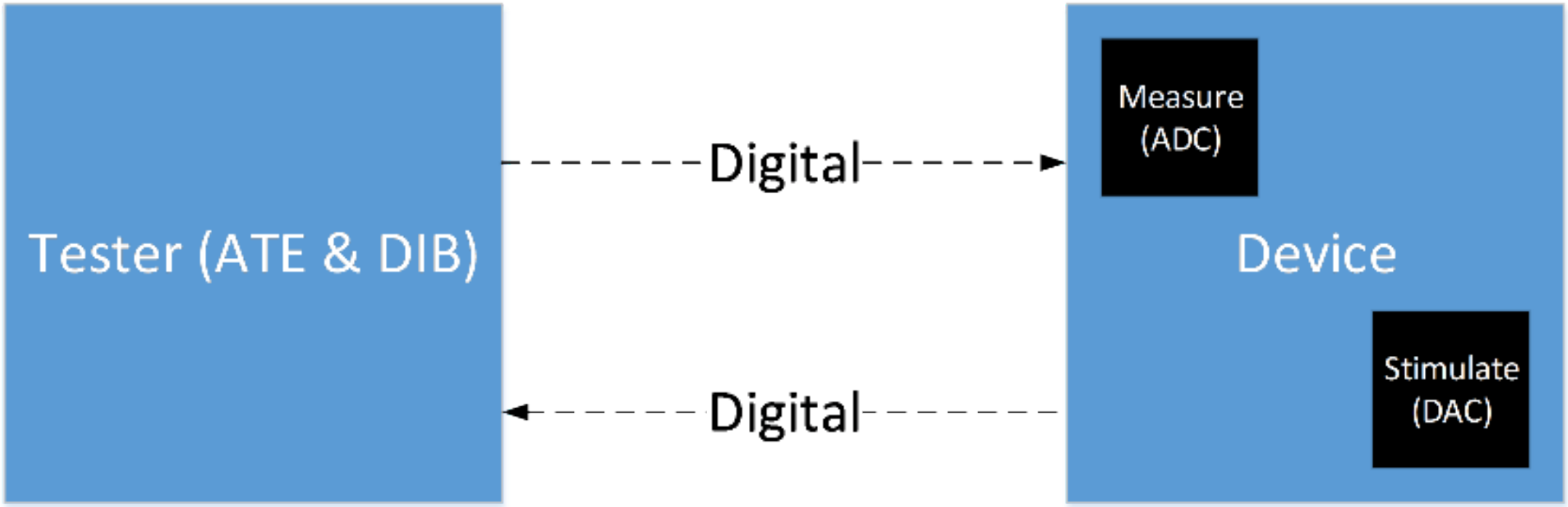


Use Model 2

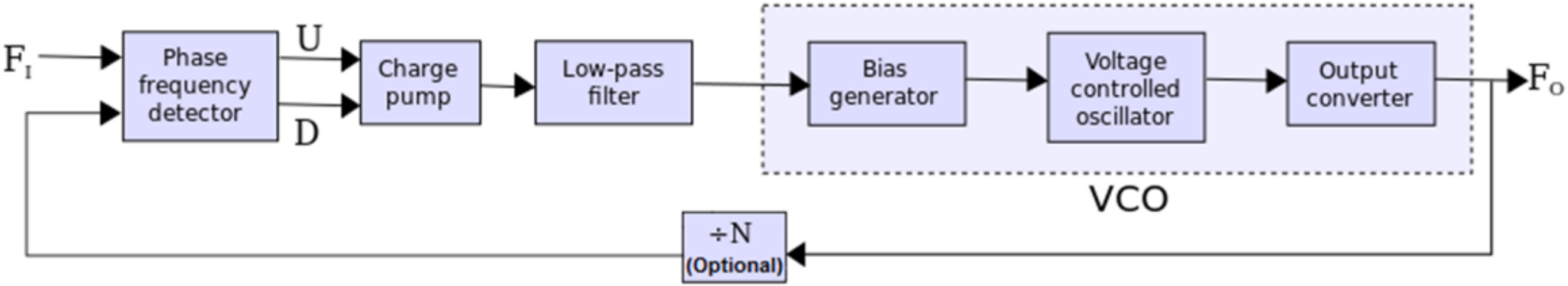
- This model has more independence from the specific ATE due to more digital capability.
  - **But still requires analog signals.**

  - As in the Use Model 1, it would be highly desirable for the ATE to provide procedures for typical ATE source/measure statements
    - i.e. ICL connection description and PDL test code for instrument operation

Use Model 3 - Stimulus & Response are digital



Use Model 3 - Example

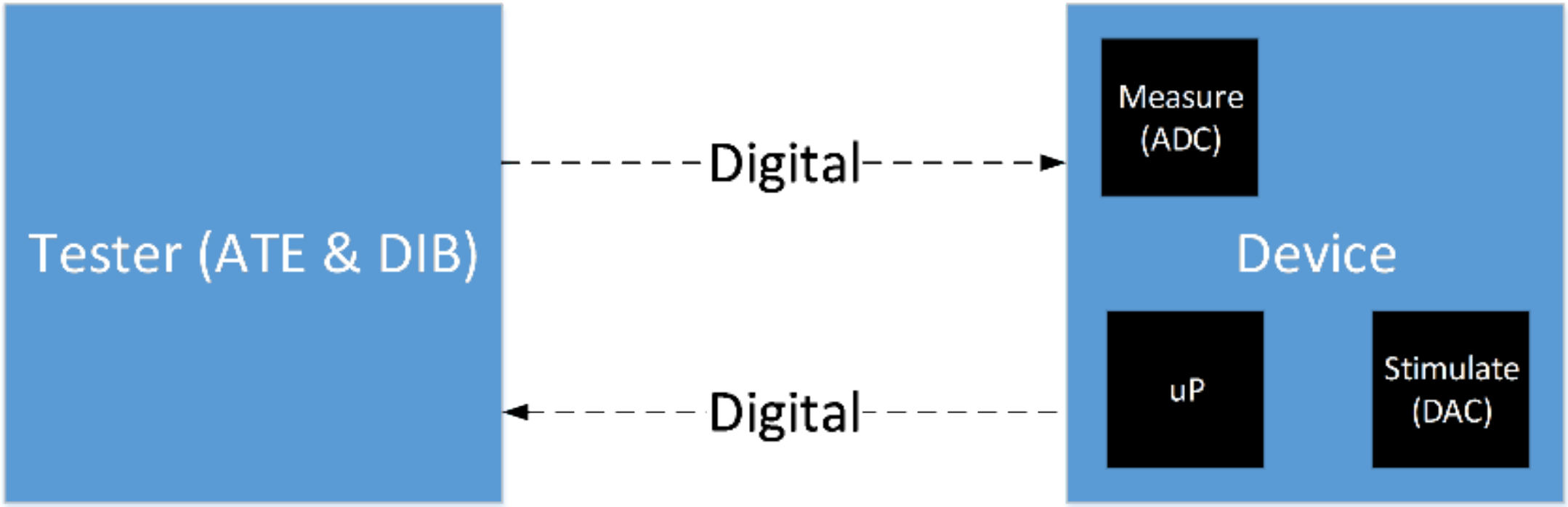


Use Model 3 - Example

- One digital input and one digital output but huge amount of analog circuitry in between.
- PLLs have measurement instruments that produce digital outputs
  - **These are perfectly suited for use with IEEE 1687.**

- This ATE use model is purely digital and the tests can be written in a portable (tester-independent) manner using PDL.

Use Model 4 – Model 3 with Intelligence



Use Model 4 – Model 3 with Intelligence

- Having a BIST onboard could allow
  - Reduced test data volume and associated test time when BIST is employed
  - Other tests may be performed concurrently while the analog self-test is underway
  - **ATE can be less complex and therefore significantly cheaper**

New PDL Commands - iForce

- iForce instead of iWrite
  - With addition arguments, "iForce I_in 10 mA" or "iForce ADC_in 1.2 V 1.0e3 Hz" would cover DC current stimulus and AC voltage stimulus, respectively.

New PDL Commands - iMeasure

- iMeasure instead of iRead
  - "iMeasure DAC_out 1V 1kHz" would cover DC current response and AC voltage response, respectively.
  - With an expected range to give a pass/fail result

New PDL Commands – Real Number & Units

- PDL has no concept of analog values, for (A)PDL
  - iForce & iMeasure commands need to contain two parts :-
  - a numerical portion
  - unit of measurement
  - i.e. 10 mV as in standard within ATE equipment

New PDL Commands – iStream

- iStream should be implemented for fast and efficient simultaneous access to DAC's and ADC
  - Defined by Steve Sunter, J.F. Cote and Jeff Rearick, ITC 2015

New PDL Commands – iSample

- iRunLoop and iApply are ok for coarse – e.g. wait times in ATE run time code
- For accurate pattern synchronized timing a new command is needed :-
  - iSample should be included
  - This would sample a number of clocks as would be done in an ATE digital pattern.

New PDL Commands

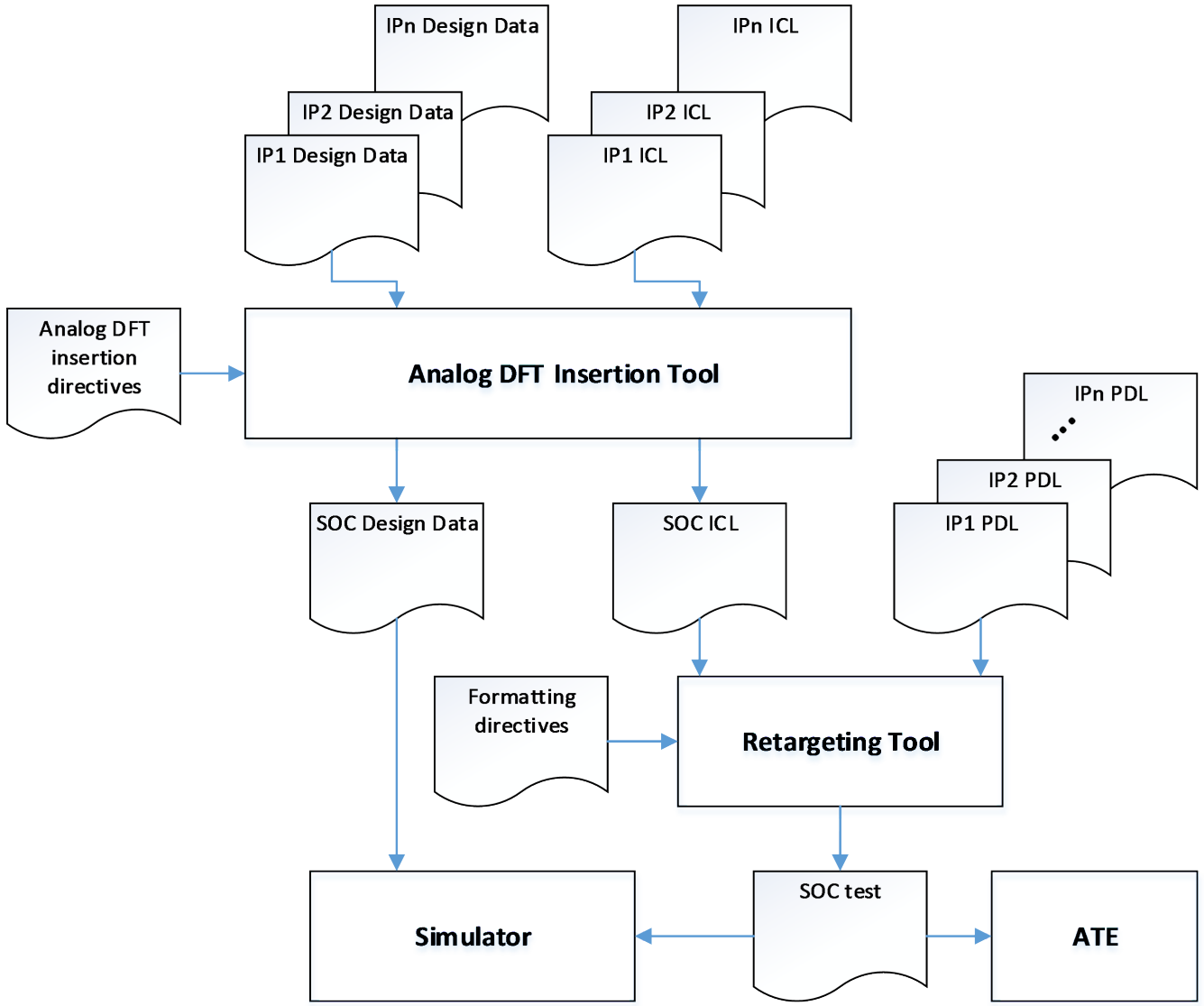
Keyword Description	New PDL Command
Keyword to specify Stimulus	iForce
Keyword to specify Response	iMeasure
Keyword for DAC/ADC wrappers	iStream
Keyword for precise wait time	iSample

ATE Extensions

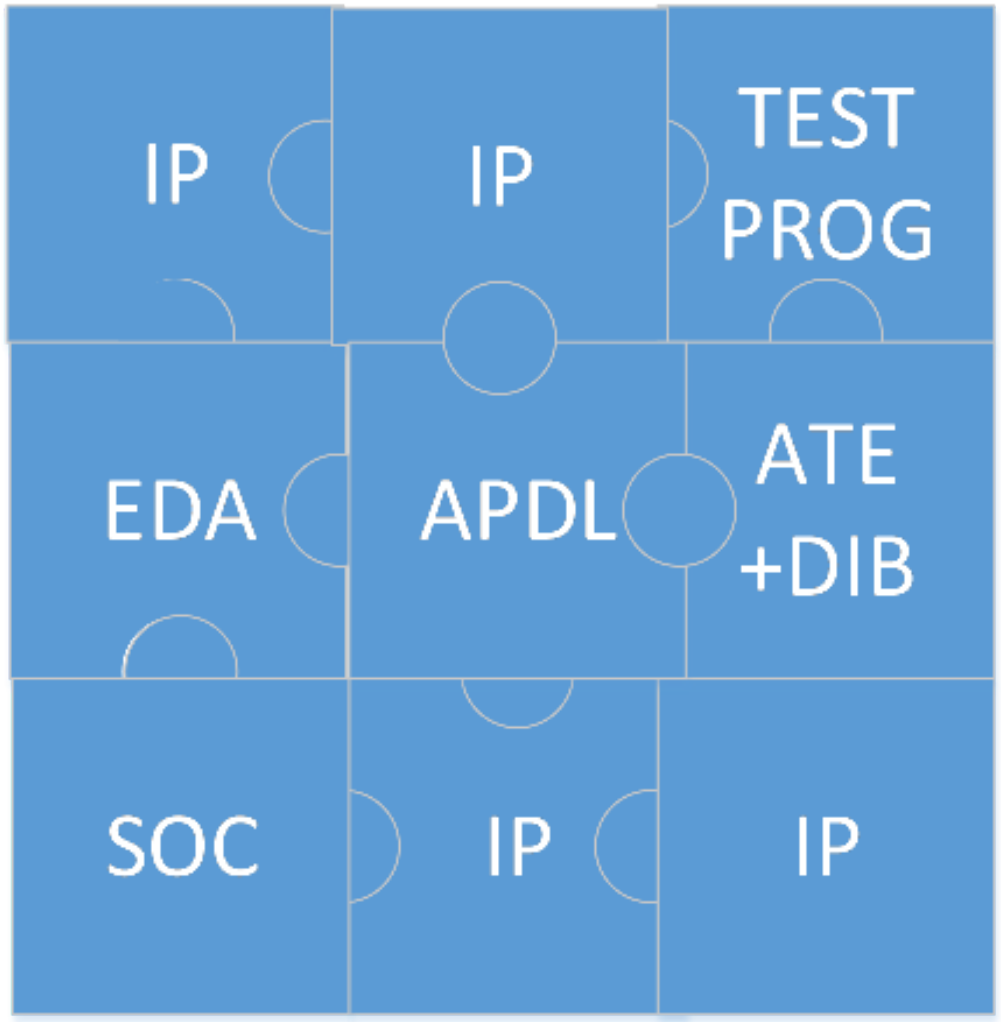
- ATE user documentation to include ICL
- iProc is a procedural call that executes a specific task on IP
- To enable 1687 on ATE
  - Creation of iProc library for ATE instrumentation
- **Having the combination of ICL and PDL of an ATE instrument will allow retargeting software to map instrument actions to the correct physical resources.**

New Ecosystem

- Envisaged Ecosystem
  - Analog DFT insertion tool
  - Retargeting Tool
  - **Output to either simulator or ATE**



1687.?? Enabled Ecosystem



IEEE Study Group

- IEEE Study Group for Analog Test Access and Coverage was established in July 2017
  - **If you would like to participate please email me at peter.sarson@ams.com for an invitation.**
- Goal is to complete 2 Project Authorization Requests to become 2 Working Groups by Q1 2018,
  - Analog Test Access
  - Analog Fault Modeling

Conclusion

- 4 use models have identified specific interactions between ATE and AMS circuits.
  - Shows that 1687 can serve as structured approach to Analog DFT
- 18 recommendations for the improvement of the ICL and PDL
- Recommendations for new practices of ATE providers and instrument designers