P2416

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Type of Project: Revision to IEEE Standard 2416-2019
Project Request Type: Initiation / Revision
PAR Request Date: 28 Oct 2019
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PAR Expiration Date: 31 Dec 2024
PAR Status: Active
Root Project: 2416-2019

1.1 Project Number: P2416
1.2 Type of Document: Standard
1.3 Life Cycle: Full Use

2.1 Project Title: Standard for Power Modeling to Enable System-Level Analysis
Change To Title: ~~IEEE~~ Standard for Power Modeling to Enable System-Level Analysis

3.1 Working Group: Power Modeling: Standard for Enabling System Level Analysis(C/DA/System Level Power Modeling)
3.1.1 Contact Information for Working Group Chair:
Name: Nagu Dhanwada
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3.1.2 Contact Information for Working Group Vice Chair:
None
3.2 Society and Committee: IEEE Computer Society/Design Automation(C/DA)
3.2.1 Contact Information for Standards Committee Chair:
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3.2.2 Contact Information for Standards Committee Vice Chair:
None
3.2.3 Contact Information for Standards Representative:
None

4.1 Type of Ballot: Entity
4.2 Expected Date of submission of draft to the IEEE SA for Initial Standards Committee Ballot: Dec 2022
4.3 Projected Completion Date for Submittal to RevCom: Oct 2023

5.1 Approximate number of entities expected to be actively involved in the development of this project: 6
5.2 Scope of proposed standard: This standard describes a parameterized and abstracted power model enabling system, software, and hardware intellectual property (IP)-centric power analysis and optimization. It defines concepts for the development of parameterized, accurate, efficient, and complete power models for systems and hardware IP blocks usable for system power analysis and optimization. These concepts include, but are not limited to, process, voltage, and temperature (PVT) independence; power and thermal management interface; and workload and architecture parameterization. Such models are suitable for use in software development flows and hardware design flows, as well as for representing both pre-silicon-estimated and post-silicon-measured data. This standard also defines the necessary requirements for the information content of parameterized, accurate, efficient, and complete power models to help guide development and usage of other related power, workload, and functional modeling standards, such as UPF IEEE Std 1801(TM)-2018, SystemC IEEE Std 1666(TM)-2016, and SystemVerilog IEEE Std 1800(TM)-2017. Beyond defining the concepts and related standard requirements, this standard also recommends the use of other relevant design flow standards (e.g., IP-XACT IEEE Std 1685(TM)-2014 [B2]2), with the objective of enabling more complete and usable power-aware design flows.
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development flows and hardware design flows, as well as for representing both pre-silicon-estimated and post-silicon-measured data. This standard also defines the necessary requirements for the information content of parameterized, accurate, efficient, and complete power models to help guide development and usage of other related power, workload, and functional modeling standards, such as UPF IEEE Std 1801(TM)-~~2015~~ 2018, SystemC IEEE Std 1666(TM)-~~2011~~ 2016, and SystemVerilog IEEE Std 1800(TM)-~~2012~~ 2017. Beyond defining the concepts and related standard requirements, this standard also recommends the use of other relevant design flow standards (e.g., IP-XACT IEEE Std 1685(TM)-2014 [B2]2), with the objective of enabling more complete and usable power-aware design flows.

5.3 Is the completion of this standard contingent upon the completion of another standard? No
5.4 Purpose: This standard supports the ability to develop accurate, efficient, and interoperable power models for complex designs, to be used with a variety of commercial products throughout an electronic system design, analysis, and verification flows.
5.5 Need for the Project: The increasing importance of power issues has spawned an interest in power-aware design flows. The problem of energy efficient system design cannot be solved in isolation, and needs to be addressed holistically. All use contexts--as seen from the point of view of software developers, system architects and reliability engineers--must be considered. Parameterized power models are a key piece of enabling such comprehensive, energy efficient systems.
These models should accurately reflect power dependence on workload and be usable for early power estimation. In particular, using existing modeling capabilities, it is very difficult to create accurate (good predictability of the amount and type of power consumed) and complete (all power events represented) power models for IP block designs which exhibit more than simple power behavior. Besides the needs of accuracy, completeness and conciseness, for any power model to be effective it must be transportable between applications that operate at different levels of abstraction (such as software programming, pre-design estimation, TLM simulation, RTL simulation, etc.), and it must address power variability issues by supporting PVT independence and power contributor segregation. Finally, the modeling techniques should be usable across different types of semiconductor IP. While some power modeling capabilities exist today, they are mainly geared for modeling low-level primitives, and are insufficient for modeling more complex objects that make up SoCs, and complete systems that may include software. These issues, among others, motivate the need for development of new standards for modeling IP blocks and entire systems; models with a sufficient level of accuracy and flexibility in order to be useful in a comprehensive power-aware design flow.
When proposing power modeling standards, related areas of use and design steps relevant to each domain must be considered. Isolated, power-aware standards exist, but none are designed to address power awareness comprehensively. Because of the inter-relationships between these different domains, and pre-existence of some standards in each, it is best to begin with a syntax-agnostic path, and focus on developing semantic aspects of these parameterized power models--models enabling comprehensive, energy efficient systems.
During the development of the 2416-2019 standard the working group had discovered a few areas where enhancements would be needed to help make the standard more robust. A few examples of these are 1) analog / mixed signal extensions, 2) robust interfacing to 1801 standards, 3) efficient handling of multi voltage designs. There were other aspects which were discovered while using the standard in prototype tools which we would like to revise in a subsequent update.
Hence, to enhance certain modeling use cases and improve efficiency of using the standard, we would like to request a revision of the standard.
5.6 Stakeholders for the Standard: communications),
* Embedded software and firmware developers,
* Software application developers,
* System Architects,
* Reliability Engineers,
* Device integrators,
* Processor providers (e.g., servers and laptops),
* Silicon vendors and manufacturers,
* Providers of semiconductor intellectual property (pre-designed blocks),
* Vendors of electronic design automation software.

All of the above stakeholders have a vested interest in the development of industry standard power modeling approaches to enable system, software and hardware IP centric power analysis and optimization.

6.1 Intellectual Property
6.1.1 Is the Standards Committee aware of any copyright permissions needed for this project? No
6.1.2 Is the Standards Committee aware of possible registration activity related to this project? No

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7.1 Are there other standards or projects with a similar scope? No
7.2 Is it the intent to develop this document jointly with another organization? No

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8.1 Additional Explanatory Notes : IEEE Std 1666 Standard for Standard SystemC Language Reference Manual (undated because it is currently under revision)
IEEE Std 1685-2014 Standard for IP-XACT, Standard Structure for Packaging, Integrating, and Reusing IP within Tool Flows
Language
IEEE Std 1801-2018 Standard for Design and Verification of Low Power, Energy Aware Electronic Systems